Dynamic Systems Approach to Improve the Design of a Phenomenological Analog Neuron Circuit

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***Abstract*—Silicon neuron circuits emulate the electrophysiological behavior of real neurons and conductances. A detailed model mapped onto silicon neuron can be beneficial to the improvement of circuit design. Here we present a dynamic systems approach to obtain a detailed mathematical model describing the dynamics of a biophysically realistic silicon neuron. The approximate analytic solution of its firing rate fits simulation data from our neuron chip fabricated using a 130 nm CMOS process very well. Meanwhile, transistors that contribute critically to variation of firing activities are discovered, which helps the improvement of neuron mismatch.**

I. Introduction

Silicon neuron circuits are one of main building elements in neuromorphic systems emulating computations carried out in the nervous system [1]. Based on the leaky integrate-and-fire neuron model, a phenomenological silicon neuron proposed in [2], [3] (Figure 1) has biophysically realistic temporal dynamics. However, there is no ideal model discribing the relationship between performance and parameters of elements in the circuit. Improvements of this silicon neuron circuit by mapping the model onto neuromorphic hardware cannot be directed theoretically. Dynamic system approach can be used to designed silicon neurons with desired dynamics [4]–[7].

In this work, we deveploped a theoretical method to improve the design of this phenomenological silicon neuron according to the dynamic systems approach. We proposed a differential equation to describe the subthreshold dynamics of the membrane potential for the silicon neuron, particalarly including the influence of each transistor's size in the circuit and bias parameters to the membrane potential. Meanwhile, we simplified this differential equation to a two-stage silicon neuron model through reasonable approximation and obtained an approximate analytic solution of its firing rate for above-threshold constant input. We simulated our test chip fabricated using a 130 nm CMOS process, in which there are 4 silicion neurons with the same structure, and compared the responses from chip simulations and theoretical predictions. Comparison results demonstrated that the approximate analytic solution of the firing rate can qualitatively characterize responses of the silicon neuron. Moreover, we explored the contribution of each transistor's mismatch to the variation of the firing rate theoretically, and proposed suggestions on the mismatch reduction of the silicon neuron.

The paper is organized as follow: first, the subthreshold dynamics of the silicon neuron and the approximate analytic solution of its firing rate were introduced in the methods section; second, results from theoretical analysis and chip simulations were shown and demonstrated the rationality of our theoretical method; third, how to reduce the mismatch are suggested; finally, results were discussed and concluded in the conclusions section.

II. Materials and Methods

A. The silicon neuron circuit

The silicon neuron circuit we describe here is originally presented in [2], [3] (Figure 1). It is a phenomenological silicon neuron with bio-physically realistic temporal dynamics. It comprises four blocks: an input differential pair integrator (DPI) circuit used as a low-pass filter ($M_1 - M_3$ and C_m) [8], a spike-event generation amplifier with current-based positive feedback ($M_4 - M_8$), a spike reset block with refractory period functionality and an inverter generating a spike.

Comparing with the voltage reset mechanism and the refractory period functionality, the current integration and the current feedback are quite slow. Therefore, its subthreshold dynamics is predominantly determined by these two slow processes analyzed in the following. The input DPI circuit implements the subthreshold behaviors of the silicon neuron, such as the leaky conductance (M_3) producing exponential subthreshold dynamics, and the integration through the capacitor C_m representing the neuron's membrane capacitance. By assuming that all transistors are operated in the subthreshold domain (the weak-inversion regime) [9], the equations that characterize this circuit are:

$$\begin{aligned} I_1 &= I_{p0} r_1 e^{\frac{\kappa}{U_T}(V_{DD}-V_{thr}) - \frac{1}{U_T}(V_{DD}-V_a)} \\ I_2 &= I_{p0} r_2 e^{\frac{\kappa}{U_T}(V_{DD}-V_m) - \frac{1}{U_T}(V_{DD}-V_a)} \\ I_1 + I_2 &= I_{in} \end{aligned} \tag{1}$$

where r is the width-length ratio of corresponding transistors (W/L), I_{p0} is the transistor dark current when $r = 1$, U_T is the thermal voltage. For the sake of simplification, we assume that both subthreshold slope factors (κ_n and κ_p) of n- and p-

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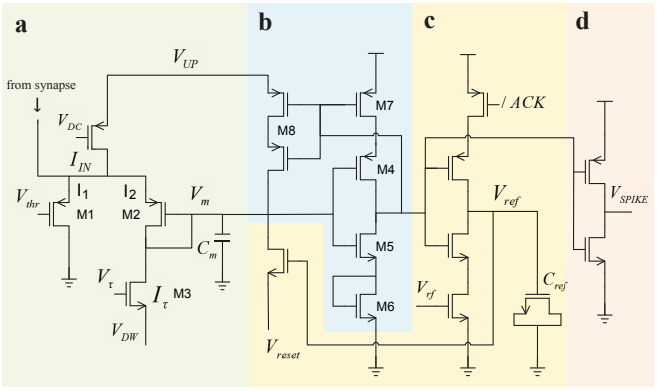

Fig. 1: **Circuit schematics of the leaky integrate-and-fire neuron** [2], [3]. **(a)** An input differential pair integrator (DPI) circuit models the neuron's leak conductance and the exponential subthreshold dynamics of the membrane potential. **(b)** An inverting amplifier with positive feedback reproduces the effect of Sodium activation and inactivation channels in real neurons. **(c)** A spike reset block with refractory period functionality realizes the reset mechanism of the membrane potential after a spike and limits the maximum activation of the neuron. **(d)** An inverter generates a short pulse (about several nanoseconds), representing a spike - the basic event of the communication between neurons.

MOSFETs here are equal to κ. From above equations, we get:

$$\mathrm{I}_S{=}\mathrm{I}_2 = \frac{I_{in}}{1+\frac{r_1}{r_2}e^{\frac{\kappa}{U_T}(V_{mem}-V_{thr})}} \approx I_{in}\frac{r_2}{r_1}e^{-\frac{\kappa}{U_T}(V_m-V_{thr})} \tag{2}$$

if V_{thr} is much smaller than V_m.

The spike-event generation amplifier with current-based positive feedback consists of transistors from M_4 - M_8. Because V_m is always much smaller than the power supply voltage V_{DD} before the spike generates, the first inverter won't be switched, which makes sure that M_5 and M_6 are operated in saturation. Therefore, the positive feedback circuit can be characterized by following equations:

$$\begin{aligned}
&M_5 : I = I_{n0}r_5 e^{\frac{\kappa}{U_T}V_m - \frac{1}{U_T}V_b}\\
&M_6 : I = I_{n0}r_6 e^{\frac{\kappa}{U_T}V_b}\\
&M_4 : I = I_{p0}r_4 e^{\frac{\kappa}{U_T}(V_{DD}-V_m)}(e^{-\frac{1}{U_T}(V_{DD}-V_d)} - e^{-\frac{1}{U_T}(V_{DD}-V_c)})\\
&M_7 : I = I_{p0}r_7 e^{\frac{\kappa}{U_T}(V_{DD}-V_c)}(1 - e^{-\frac{1}{U_T}(V_{DD}-V_d)})\\
&M_8 : I_P = I_{p0}r_8 e^{\frac{\kappa}{U_T}(V_{DD}-V_c)}
\end{aligned} \tag{3}$$

Considering that V_m is always much smaller than the power supply voltage V_{DD}, the positive feedback current I_P can be simplified further as follows:

$$I_P \approx I_{n0}\frac{r_5^{\frac{\kappa}{1+\kappa}}r_6^{\frac{1}{1+\kappa}}r_8}{r_7}e^{\frac{\kappa^2}{1+\kappa}\frac{V_m}{U_T}} \tag{4}$$

From this equation, we can conclude that the size of transistor M_4 has no influence on the positive feedback current. However, it still determines the switch threshold of this spike-event generation amplifier. According to the above analysis, the subthreshold dynamics of the membrane potential for the silicon neuron can be described by a differential equation as follows [2], [10]:

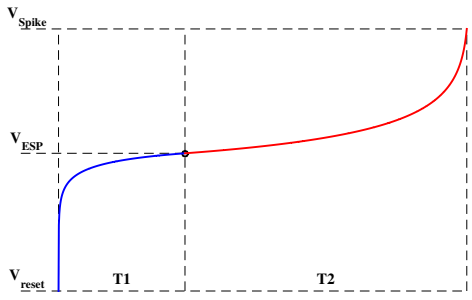

Fig. 2: The approximate analytic solution for membrane potential (V_m) of two-stage neuron circuit model in response to a constant injected current. V_{ESP} is a voltage value of V_m, at which the effective injected current I_S is equal to the positive feedback current I_P. T_1 denotes the time during which V_m evolves from the reset voltage V_{reset} to the voltage V_{ESP}, and T_2 denotes the time during which V_m evolves from V_{ESP} to V_{Spike}.

$$C_m\frac{dV_m}{dt} = I_{in}\frac{r_2}{r_1}e^{-\frac{\kappa}{U_T}(V_m-V_{thr})} - r_3I_\tau + I_{n0}\frac{r_5^{\frac{\kappa}{1+\kappa}}r_6^{\frac{1}{1+\kappa}}r_8}{r_7}e^{\frac{\kappa^2}{1+\kappa}\frac{V_m}{U_T}} \tag{5}$$

in which r_3I_τ represents the leaky current I_L through the transistor M_3.

B. The approximate analytic solution of the firing rate

For above-threshold constant input, this silicon neuron fires at a constant frequency, that is, the firing rate. However, it seems impossible to obtain the analytic solution of its firing rate according to Equation 5. So we turn to seek its approximate analytic solution. Equation 5 shows that the injected current (I_S) plays a major role in the early charge of the membrane capacitor, and later the positive feedback current (I_P) dominates the spike generation. Currents I_S and I_P are equal with each other when $V_m = V_{ESP}$. Therefore, above differential equation model can be simplified to a two-stage silicon neuron model [10], as follows:

$$\begin{cases}
C_m\frac{dV_m}{dt} = I_{in}\frac{r_2}{r_1}e^{-\frac{\kappa}{U_T}(V_m-V_{thr})} - r_3I_\tau & if \quad V_m \le V_{ESP}\\
C_m\frac{dV_m}{dt} = -r_3I_\tau + I_{n0}\frac{r_5^{\frac{\kappa}{1+\kappa}}r_6^{\frac{1}{1+\kappa}}r_8}{r_7}e^{\frac{\kappa^2}{1+\kappa}\frac{V_m}{U_T}} & if \quad V_m > V_{ESP}
\end{cases} \tag{6}$$

where

$$V_{ESP} = \frac{1+\kappa}{\kappa(1+2\kappa)}U_T\log\frac{I_{in}r_2r_7}{I_{n0}r_1r_5^{\frac{\kappa}{1+\kappa}}r_6^{\frac{1}{1+\kappa}}r_8}e^{\frac{\kappa}{U_T}V_{thr}}$$

Because a certain amount of currents have been ignored in both stage of spike generation, the response of the two-stage silicon neuron model will be lower than that of original differential equation model (Equation 5). However, it can help us to get a simple analytic solution of the firing rate and to explore how different parameters (the size of transistors, the leaky current and biased voltages) will determine the response of silicon neuron. The time course of membrane potential V_m is

shown in Figure 2. From the approximate analytic expressions of membrane potential, we get:

$$\begin{cases} T_1 \approx -\frac{C_m U_T}{\kappa I_\tau r_3} \log[1 - \frac{I_\tau r_1 r_3}{I_{in} r_2} e^{\frac{\kappa}{U_T}(V_{ESP} - V_{thr})}] \\ T_2 \approx -\frac{1+\kappa}{\kappa^2} \frac{C_m U_T}{I_\tau r_3} \log[1 - \frac{I_\tau r_3 r_7}{I_{n0} r_5^{\frac{\kappa}{1+\kappa}} r_6^{\frac{1}{1+\kappa}} r_8} e^{-\frac{\kappa^2}{1+\kappa}\frac{V_{ESP}}{U_T}}] \end{cases} \quad (7)$$

Then, by replacing V_{ESP} we get:

$$T = T_1 + T_2 = -\frac{1+2\kappa}{\kappa^2} \frac{C_m U_T}{I_\tau r_3} \log[1 - \frac{I_\tau r_1^{\frac{1}{1+2\kappa}} r_3 r_7^{\frac{1+\kappa}{1+2\kappa}}}{I_{in}^{\frac{\kappa}{1+2\kappa}} I_{n0}^{\frac{1+\kappa}{1+2\kappa}} r_2^{\frac{1}{1+2\kappa}} r_5^{\frac{\kappa}{1+2\kappa}} r_6^{\frac{\kappa}{1+2\kappa}} r_8^{\frac{1+\kappa}{1+2\kappa}}} e^{-\frac{\kappa^2}{1+2\kappa}\frac{V_{thr}}{U_T}}] \quad (8)$$

After we get the interspike interval T, the firing rate F without considering the refractory period can be described as follows:

$$F = \frac{1}{T} \quad (9)$$

According to Equation 8 and 9, the relationship between the firing rate and the injected constant current can be described as follows in a succinct way:

$$f(I_{in}) = \frac{-\frac{\kappa^2}{1+2\kappa}\frac{I_L}{C_m U_T}}{\log[1 - I_L I_{fb}^{-\frac{1+\kappa}{1+2\kappa}} e^{-\frac{\kappa^2}{1+2\kappa}\frac{V_{thr}}{U_T}} I_{in}^{-\frac{\kappa}{1+2\kappa}}]} \quad (10)$$

which reveals that the silicon neuron will not fire until the injected current is larger than $I_{th} = I_L^{\frac{1+2\kappa}{\kappa}} I_{fb}^{-\frac{1+\kappa}{\kappa}} e^{-\kappa\frac{V_{thr}}{U_T}}$. When the injected current I_{in} is controlled by the voltage V_{DC}, $I_{in} = I_{p0} e^{-\frac{\kappa}{U_T}(V_{DC} - V_{DD})}$. Thus the analytic solution of the firing rate is the function of the voltage V_{DC}:

$$f(V_{DC}) = \frac{-\frac{\kappa^2}{1+2\kappa}\frac{I_L}{C_m U_T}}{\log[1 - I_L I_{fb}^{-\frac{1+\kappa}{1+2\kappa}} e^{-\frac{\kappa^2}{1+2\kappa}\frac{V_{thr}+V_{DD}}{U_T}} I_{p0}^{-\frac{\kappa}{1+2\kappa}} e^{\frac{\kappa^2}{1+2\kappa}\frac{V_{DC}}{U_T}}]} \quad (11)$$

As we mentioned before [10], the approximate analytic solution of the firing rate is in qualitative accordance with that in numerical simulations for the differential equation (Equation 5) in the condition of small leaky current I_τ and low voltage V_{thr}. Considering Equation 11 is an approximate analytic solution of the firing rate, we used the following simplified function to fit the mean firing rate of silicon neurons on the chip:

$$f(V_{DC}) = \frac{g}{\log(1 - \theta e^{\gamma V_{DC}})} \quad (12)$$

where g, θ and γ are corresponding to the terms in Equation 11.

III. Results

We tested the responses of this silicon neuron in the chip given the constant current stimulus with different strengths biased by the voltage V_{DC} (Figure 3). When the voltage V_{DC} is high, the constant current injected to the silicon neuron is small and so the silicon neuron cannot fire (not shown). When the voltage $V_{DC} = 0.785V$ (Figure 3a), the membrane voltage V_m ramps up rapidly from the reset voltage V_{reset} due to the input

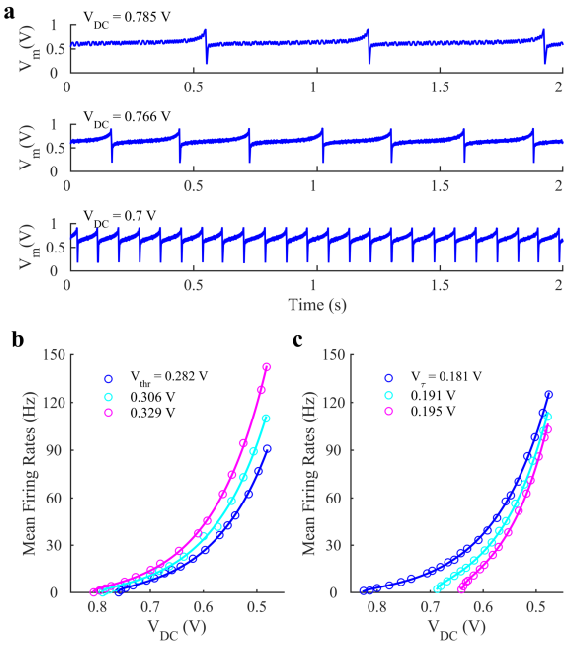

Fig. 3: **Responses of on-chip silicon neurons to constant injection currents. (a)** Membrane potential (V_m) of the silicon neuron to the increasing constant injection currents biased by the voltage V_{DC}. As the voltage V_{DC} decreases, the interspike interval also decreases, that is, the spike frequency of the silicon neuron increases. **(b-c)** The relationship between mean firing rates and the voltage V_{DC} for varying V_{thr} (**b**) and varying V_τ (**c**). Circles represent the data from simulations on the chip, while solid curves are fitted according to Equation 12. Responses of the silicon neuron are stronger for higher V_{thr} and lower V_τ.

current, and then increases slowly as the effective input current (the first term in Equation 5) becomes small. Although this effective input current decreases further with the increasing V_m, V_m still increases dramatically due to the positive feedback current (the third term in Equation 5) at the later period of a spike. As the voltage V_{DC} decreases, the interspike interval also decreases, which indicates the corresponding firing rate increases. Figure 3b and 3c show relationships between mean firing rates of the silicon neuron and the voltage V_{DC}. The data represented by circles are the statistical results from the experimental data of the chip simulations. The silicon neuron doesn't fire until the voltage V_{DC} is lower than a certain value called the threshold voltage V_{th}, and then its mean firing rate rises gradually with the decreasing of the voltage V_{DC}.

The voltage V_{thr} and V_τ configure the gain and the leaky current of the silicon neuron, respectively. For a given voltage V_{DC}, mean firing rates of the silicon neuron and its gain increase with the increasing voltage V_{thr} (Figure 3b), but decrease with the voltage V_τ (Figure 3c). Meanwhile, the threshold voltage V_{th} increases with the voltage V_{thr} (Figure 3b) and decreases with the voltage V_τ (Figure 3c). In order to check the approximate analytic solution of the firing rate we proposed (Equation 11), we used a fitting function (Equation 12) to fit the experimental data. Although the silicon neuron circuit on the chip and the fitting function don't use the same

set of biased voltages, they almost agree with each other (Figure 3b and 3c). Above results demonstrate the approximate analytic solution of the firing rate can qualitatively characterizes responses of the silicon neuron.

IV. Improvement for the Mismatch

In this section, we explored reduction of mismatch for silicon neurons based on our approximate analytic solution of the firing rate.

The general behavior of drain current of transistor in saturation can be described by an approximative model, which sacrifice accuracy to clarity and simplicity:

$$\begin{aligned} I_D &= I_0 e^{\frac{V_{GS}}{U_T}} \\ I_0 &= \mu C_{ox} U_T^2 \frac{W}{L} e^{-\frac{V_{T0}}{U_T}} \end{aligned} \tag{13}$$

where V_{T0} is the threshold voltage of the transistor, and C_{ox} is the oxide capacitance per unit area [9], [11]. I_0 denotes the dark current of the transistor already including the parameter r (W/L). When transistors have the same gate voltage and operate in weak inversion, the mismatch of their drain currents is

$$\sigma^2(\frac{\Delta I_D}{I_D}) = (\frac{g_m}{I_D})^2 \sigma^2(\Delta V_{T0}) = \frac{1}{U_T^2}\sigma^2(\Delta V_{T0}) = \frac{A_{vt}^2}{U_T^2}\frac{1}{S} \tag{14}$$

where the parameter g_m is the transconductance of transistors, A_{vt} is a technology-dependent parameter, and S is the area of the transistor [12]–[14]. According to the relationship between I_D and I_0, we can further get:

$$\sigma^2(\Delta I_0) = \frac{I_0^2 A_{vt}^2}{U_T^2}\frac{1}{S} \tag{15}$$

In order to investigate MOSFET mismatch for the response of silicon neuron, we rewritten the analytic formula of the firing rate $(F = \frac{1}{T})$ including parameters $I_{0i}, i = 1,2,...8$ as follows:

$$T = -\frac{1+2\kappa}{\kappa^2}\frac{C_m U_T}{I_{03} e^{\frac{\kappa}{U_T}V_\tau}} \log[1 - \frac{I_{01}^{\frac{1}{1+2\kappa}} I_{03} I_{07}^{\frac{1+\kappa}{1+2\kappa}}}{I_{in}^{\frac{1+\kappa}{1+2\kappa}} I_{n0}^{\frac{1-\kappa}{1+2\kappa}} I_{02}^{\frac{1}{1+2\kappa}} I_{05}^{\frac{\kappa}{1+2\kappa}} I_{06}^{\frac{\kappa}{1+2\kappa}} I_{08}^{\frac{1+\kappa}{1+2\kappa}}} e^{\frac{\kappa}{U_T}V_\tau} e^{-\frac{\kappa^2}{1+2\kappa}\frac{V_{thr}}{U_T}}] \tag{16}$$

where V_τ is bias voltage of M_3 responsible for the leaky current. Here for the sake of simplification, we also define:

$$B(I_{01}, I_{02}, \cdots, I_{08}) = \frac{I_{01}^{\frac{1}{1+2\kappa}} I_{03} I_{07}^{\frac{1+\kappa}{1+2\kappa}}}{I_{in}^{\frac{1+\kappa}{1+2\kappa}} I_{n0}^{\frac{1-\kappa}{1+2\kappa}} I_{02}^{\frac{1}{1+2\kappa}} I_{05}^{\frac{\kappa}{1+2\kappa}} I_{06}^{\frac{\kappa}{1+2\kappa}} I_{08}^{\frac{1+\kappa}{1+2\kappa}}} e^{\frac{\kappa}{U_T}V_\tau} e^{-\frac{\kappa^2}{1+2\kappa}\frac{V_{thr}}{U_T}} \tag{17}$$

Therefore, the influence of I_0 of each transistor on the firing rate can be described in the following way:

$$\frac{\partial F}{\partial I_{0i}} = -\frac{1+2\kappa}{\kappa^2}\frac{C_m U_T}{I_{03} e^{\frac{\kappa}{U_T}V_\tau}}\frac{BF^2}{1-B}\frac{1}{I_{0i}}x_i \tag{18}$$

where x_i in the above equation is the power of I_{0i} in the expression $B(I_{01},...,I_{08})$ except I_{03} and I_{04} as shown in Table I. Combining all analysis above, the mismatch of the firing rate for the silicon neuron is given by the following equation:

$$\begin{aligned} \sigma^2(\Delta F) &= \sum_{i=1}^{8} (\frac{\partial F}{\partial I_{0i}})^2 \sigma^2(\Delta I_{0i}) \\ &= F^4 A_{vt}^2 (\frac{1+2\kappa}{\kappa^2}\frac{C_m U_T}{I_{03} e^{\frac{\kappa}{U_T}V_\tau}}\frac{B}{1-B})^2 \sum_{i=1}^{8}\frac{x_i^2}{S_i} \end{aligned} \tag{19}$$

TABLE I: Values of x_i

x_1	x_2	x_3	x_4
$\frac{1}{1+2\kappa}$	$-\frac{1}{1+2\kappa}$	$1-(1-\frac{1}{B})log(1-B)$	0
x_5	x_6	x_7	x_8
$-\frac{\kappa}{1+2\kappa}$	$-\frac{\kappa}{1+2\kappa}$	$\frac{1+\kappa}{1+2\kappa}$	$-\frac{1+\kappa}{1+2\kappa}$

If we have enough space on the chip, one effective way to reduce the mismatch is to increase the size of all transistors S_i. However, if the total area of all transistors is limited, reducing the mismatch of silicon neuron becomes a standard optimization problem as follows:

$$\begin{cases} minimize \quad (S_i) \quad \sigma^2(\Delta F) = F^4 A_{vt}^2 (\frac{1+2\kappa}{\kappa^2}\frac{C_m U_T}{I_{03} e^{\frac{\kappa}{U_T}V_\tau}}\frac{B}{1-B})^2 \sum_{i=1}^{8}\frac{x_i^2}{S_i} \\ subject \quad to \qquad\qquad \sum_{i=1}^{8} S_i = S_{tot} \end{cases} \tag{20}$$

In order to minimize $\sigma^2(\Delta F)$, their area proportions should be consistent with the ratio of $x_i^2, i \neq 4$ (Table I). Therefore, the size S_3 of the transistor that sets the neuron's leak time constants should be considered mostly becasue x_3 will become very large when the silicon neuron fires with the low frequency. Similarly, the priority of remaining transistors' sizes we consider is $x_{7,8}$, $x_{1,2}$ and $x_{5,6}$. Other transistors in the circuit are not major contributors to neuron's mismatch and don't need to be considered too much.

V. Conclusions

In this study, we constructed a detailed mathematical model to describe the subthreshold dynamics of silicon neuron, which is similar to the silicon neuron model by Livi [2]. The approximate analytic solution of its firing rate fits simulation data from our neuron chip fabricated using a 130 nm CMOS process very well, the fact of which demonstrates the rationality of our detailed model. Furthermore, considering inevitable errors of 'identical' devices, we also do the mismatch analysis to explore the contribution of each transistor's mismatch to the variation of the firing rate [15], [16], and then conclude that maintaining the optimal ratio of several critial transistors' sizes can effectively reduce the mismatch of silicon neuron. However, we still need to consider some tradeoffs, involving the mismatch, the speed of the circuit, the limitation of the area for single neuron circuit, the layout of all transistors and routings.

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